# Designing a Graphic Equalizer

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E E 433
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# Abstract

This report details the design process and testing of a 7-band graphic equalizer with bands from 100 Hz to 6.4 kHz with a gain of 6 V/V. This project details the circuit analysis for the equalizer and the gyrator filter elements, discussing design choices and ways to improve on our design. The circuit is then built and tested against expected results.

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# Introduction

In this report, we will describe the design and testing process for a seven-band graphic equalizer. The design we chose is an LCR configuration equalizer. We will also derive equations for a simulated inductor active filter, and implement them in the filter design. We will also provide the specifications our design is designed upon, different designs we went through in our design procedure, and the test results and analysis of our finalize equalizer. We will then discuss various aspects of our design and the tradeoffs for our design choices. Finally, we will describe ways to improve on our design to beter meet the design specifications.

# Design Specification

The design of the equalizer must be seven bands with center frequencies at 100, 200, 400, 800, 1600, 3200, and 6400Hz with octave bandwidths. Each band must have a variable gain from 0V/V to 6V/V. The overall equalizer must be able to function at a supply rail of ±12 volts. These requirements must be met with minimum parts and power consumption as possible. The design also has to be capable of cancelling any DC offset in the input signal.

# Design Procedure

## *Band-gap filters*

Our equalizer consisted of seven band-gap filters with center frequencies at 100 Hz, 200 Hz, 400 Hz, 800 Hz, 1.6 kHz, 3.2 kHz, and 6.4 kHz. To create these filters, we needed to incorporate seven band-pass filters such as the RLC series circuit, shown in Figure 1. In this filter, we have an inductor, capacitor, and resister in series. To find the input impedance of this filter, we add up all the impedances of the individual elements:

$$Z_{in}(s) = R + sL + \frac{1}{sC}$$

$$\rightarrow Z_{in}(s) = \frac{s^2 + s\frac{R}{L} + \frac{1}{LC}}{sC}$$

*Equation 1*

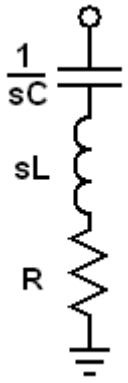


*Figure 1. RLC circuit*

To find the center frequency for this circuit, we take the derivative of the input impedance with respect to$\omega$, set the derivative to 0, and solve for $\omega_0$:

$$\frac{d}{d\omega}\left(R + j\omega L - \frac{j}{\omega C}\right) = j\left(L + \frac{1}{\omega^2 C}\right) = 0$$

$$\rightarrow \omega_0 = \frac{1}{\sqrt{LC}}$$

*Equation 2*

The bandwidth ($\Delta\omega$) for the RLC filter is R/L (see equation 1). The Q factor is then $\omega_0$ divided by the bandwidth:

$$Q = \frac{\omega_0}{\Delta\omega} = \frac{L}{R\sqrt{LC}} = \frac{1}{R}\sqrt{\frac{L}{C}}$$

*Equation 3*

Based on equations 2 and 3, we can now solve for the inductor and capacitor values to make our LRC filters for the equalizer circuit if we were to use only passive elements.

## *Simulated Inductor Circuit*

The simulated inductor circuit (or 'gyrator' circuit) is useful for simulating inductors. Since inductors are usually bulky and expensive, it is preferable to use active filters with op-amps. Figure 2 shows a band-reject filter implementing a simulated inductor.

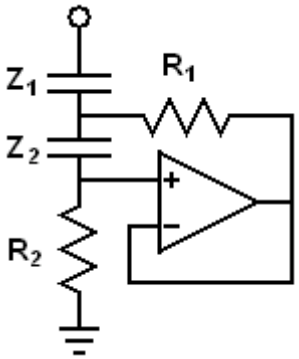


*Figure 2. Gyrator filter*

To understand the operation of this circuit, we can use circuit analysis to derive equations for the input impedance for the circuit. Assuming an ideal op-amp, we will note that the voltages at all pins are the same on the op-amp, which we will call $V_{out}$. We will label the node between the capacitors *A* and the voltage at that node $V_A$, and assume the input voltage is 1 volt. The Kirchhoff Current Law equations for this circuit at nodes *A* and the non-inverting op-amp pin are as follows:

$$\frac{V_A - 1}{Z_1} + \frac{V_A - V_{out}}{R_1} + \frac{V_A - V_{out}}{Z_2} = 0$$
$$\frac{V_{out} - V_A}{Z_2} + \frac{V_{out}}{R_2} = 0 \qquad \textit{Equation 4}$$

After algebraic manipulation, we can come up with the following solution for the value of $V_A$:

$$V_A = \frac{R_1(R_2 + Z_2)}{R_1Z_1 + R_1R_2 + Z_1Z_2 + R_1Z_2} \qquad \textit{Equation 5}$$

Since we know the voltage at node *A*, we can solve for the current through the capacitor $Z_1$:

$$I_{Z2} = \frac{R_1 + Z_2}{R_1Z_1 + R_1R_2 + Z_1Z_2 + R_1Z_2} \qquad \textit{Equation 6}$$

Since we assumed an input voltage of one volt, equation 6 is also $1/Z_{in}$. We can now we can solve for the transfer function for the gyrator circuit by substituting $Z_1=1/sC_1$ and $Z_2=1/sC_2$. The transfer function is as follows:

$$Z_{in}(s) = \frac{s^2 + s\frac{C_1 + C_2}{R_2C_1C_2} + \frac{1}{R_1R_2C_1C_2}}{s^2\frac{1}{R_2} + s\frac{1}{R_1R_2C_2}} \qquad \textit{Equation 7}$$

Equation 7 has a second order term in the denominator that does not show up in the transfer function of the RLC circuit (see equation 1). At high enough frequencies, this term will begin to dominate, causing unwanted high-frequency filtering. If the value of $R_2$ is made too small, the high frequency effects will begin at lower frequencies. For this reason, we prefer the value of $R_2$ to be as high as possible.

Since the value of $R_2$ is a finite value, the filters will all suffer from high frequency effects. The gyrator circuit will be ineffective for very large frequencies because as $\omega$ gets large, the $s^2$ term in the denominator of equation 7 dominates, and the circuit no longer acts as a band-reject filter but a low-pass filter. Although for these filters, the high frequency effects don't begin to take place until well after 10 kHz, which is outside the intended range of use for the equalizer circuit. Therefore, for the purposes of this design, we will ignore the $s^2$ term.

Substituting in $s = j\omega$, we can derive the phasor equivalent.

$$Zin(\omega) = R_1 + \frac{R_1 C2}{C1} + j\left(\omega R_1 R_2 C_2 - \frac{1}{\omega C1}\right) \quad \textit{Equation 8}$$

If we ignore the second order term in the denominator of equation 7, we can approximate the values of Q and $\omega_0$. These values are:

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\Delta\omega = \frac{C_1 + C_2}{R_2 C_1 C_2} \quad \textit{Equation 9}$$

$$Q = \frac{\omega_0}{\Delta\omega} = \frac{R_2 C_1 C_2}{(C_1 + C_2)\sqrt{R_1 R_2 C_1 C_2}}$$

$$\rightarrow Q = \frac{1}{C_1 + C_2}\sqrt{\frac{R_2 C_1 C_2}{R_1}}$$

We can achieve a large value of $R_2$ by making $C_1$ a much higher value than $C_2$. For this reason, we specified that C1 be 1000 times the value of C2. Now we can solve for the actual component values of the gyrator circuit as a function of Q and $\omega_0$:

$$C_1 = -\frac{1000}{1001\,\omega_0\,Q\,R_1}$$

$$C_2 = \frac{C_1}{1000} \quad \textit{Equation 10}$$

$$R_2 = \frac{1002001}{1000} R_1 Q^2$$

For reasons we will discuss later, we chose that $R_1$ be equal to 100 Ω. Based on equation 9, we now have enough information to determine all resistor and capacitor values for our gyrator circuit. Table 1 lists the component values for our filters for Q = $\sqrt{2}$ .

| ***f*** **(Hz)** | **R1** | **R2** | **C1** | **C2** |
|---|---|---|---|---|
| 100 | 100 Ω | 200 kΩ | 11.24 μF | 11.24 nF |
| 200 | 100 Ω | 200 kΩ | 5.62 μF | 5.62 nF |
| 400 | 100 Ω | 200 kΩ | 2.81 μF | 2.81 nF |
| 800 | 100 Ω | 200 kΩ | 1.41 μF | 1.41 nF |
| 1600 | 100 Ω | 200 kΩ | 703 nF | 703 pF |
| 3200 | 100 Ω | 200 kΩ | 351 nF | 351 pF |
| 6400 | 100 Ω | 200 kΩ | 176 nF | 176 pF |

*Table 1. List of component values for each active filter in the equalizer circuit*

Figure 3 shows a plot of the current through a 100 Hz filter by a RLC circuit and a gyrator circuit when applying an AC voltage of magnitude 1 volt. Notice the two graphs are very similar until 10 kHz, where the higher order term in the denominator of equation 7 begins to dominates, and the resistance seen through the gyrator circuit drops.

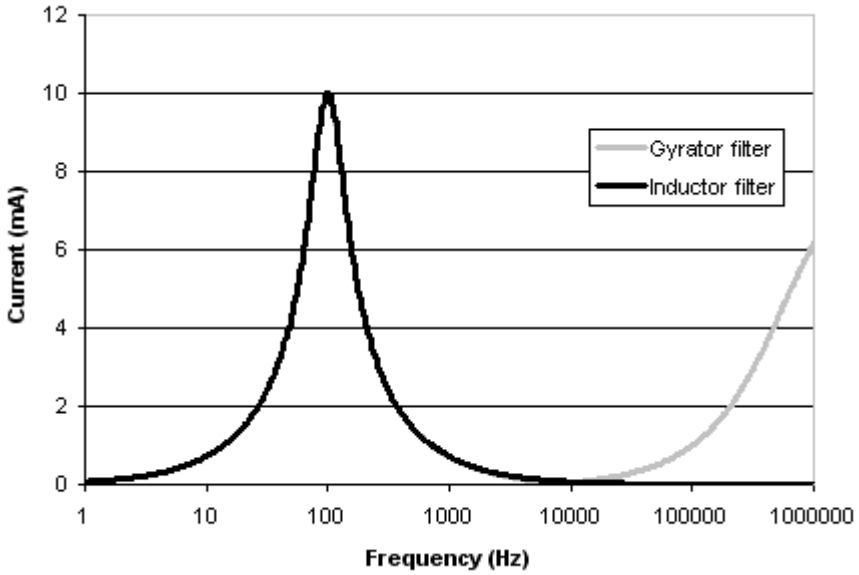


*Figure 3. Frequency response of RLC filter compared to a gyrator filter*

For the circuit to be used for higher frequency applications, we would need to incorporate first-order filtering to counteract the high frequency effects of the gyrator circuit. For the purposes of this project, we will assume the circuit is only to be used for frequencies less than 10 kHz.

## *Filter Configuration*

After designing the filters, we connected them in parallel with a configuration shown in Figure 4[1]. Using this configuration, we are able to apply a boost or a cut to the signal depending on the state of the potentiometer. By varying a potentiometer, we would affect whether the filter provides a boost or a filter for that frequency.

[1] Greiner & Schoessow, p. 402 – Configuration 3

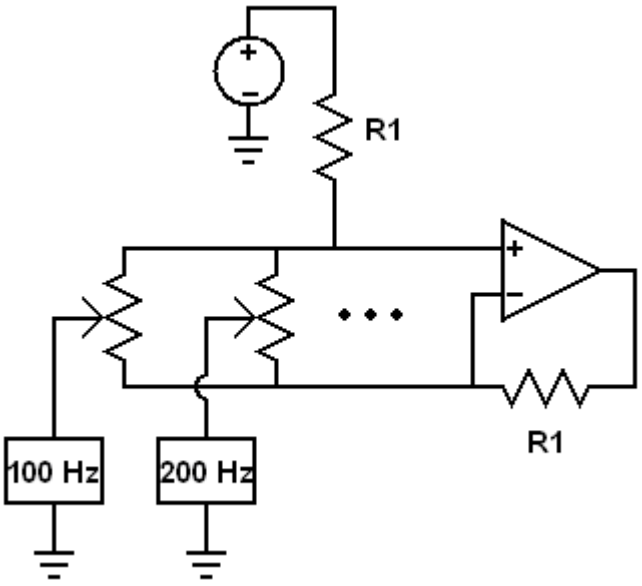


*Figure 4. Filter configuration for equalizer circuit*

When we plug the cutoff frequency into the transfer equation for the gyrator circuit (equation 7) and ignore the $s^2$ term in the denominator, we can calculate the minimum resistance seen through the filter at the frequency of resonance:

$$Z_{in}(\omega_0) = R_1 + \frac{R_1 C2}{C1} + j\left(\frac{1}{\sqrt{R_1 R_2 C_1 C_2}} R_1 R_2 C_2 - \frac{1}{\frac{1}{\sqrt{R_1 R_2 C_1 C_2}} C1}\right) \qquad \textit{Equation 11}$$

$$\rightarrow Z_{in}(\omega_0) = R_1\left(1 + \frac{C_2}{C_1}\right)$$

Earlier, we specified that $C_1 = 1000\ C_2$. For that reason, we can ignore the term $C_2/C_1$ in equation 11 since it is very small, and approximate the input impedance at the cutoff frequency as $R_1$.

From equation 11, we find that at the resonant frequency of the filter elements, the resistance seen through the filter can be modeled by the value of $R_1$, which we set to 100 Ω for all our filter elements. By modeling a filter by a single resister, we can solve for the gain provided to each filter at its resonant frequency.

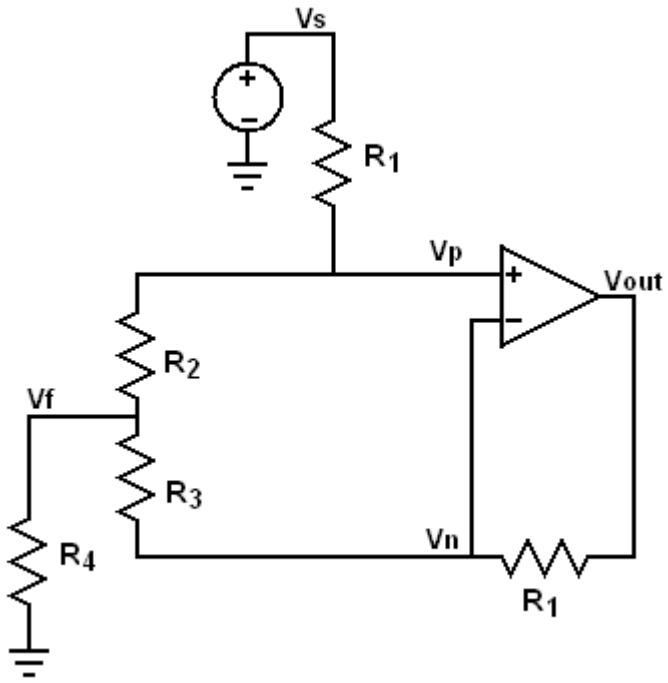


*Figure 5. Simplified equalizer circuit with one filter modeled at cutoff frequency for individual band*

With the circuit in Figure 5, we can derive a transfer function involving $V_s$ and $V_{out}$. The resulting equation is:

$$\frac{V_{out}}{V_s} = \frac{R_1R_2 + R_2R_3 + R_2R_4 + R_3R_4}{R_1R_3 + R_2R_3 + R_2R_4 + R_3R_4} \qquad \textit{Equation 12}$$

When we vary the potentiometer to its extremes, we in effect remove R2 and R3 from the equation depending on which way we turn the potentiometer.

$$\left.\frac{V_{out}}{V_s}\right|_{R2=0} = \frac{R_4}{R_1 + R_4} \quad \text{(min gain)}$$

$$\left.\frac{V_{out}}{V_s}\right|_{R3=0} = \frac{R_1 + R_4}{R_4} \quad \text{(max gain)} \qquad \textit{Equation 13}$$

For all the filters in the circuit to have the same maximum and minimum gain, the values of R4 for all the filters has to be the same value. For this reason, we specified all the resistors be equal to 100 Ω. Using this value, we need a resistor value of 500 Ω for $R_1$ in order to achieve a gain of 6 based on equation 12. Since resistors don't come in 500 Ω denominations, we selected a value of 510 Ω. Therefore, the gain values for our circuit vary from 0.16 and 6.1.

Unfortunately, this ideal model with only one filter doesn't account for parallel resistances caused by other filters, which though not at their peak, still have a small resistance. This causes the gain of the filter

to drop significantly, and causes an uneven gain distribution among the filters. The 100 Hz and 1600 Hz filters, which only have neighboring filters on one side, are least affected by this filtering, and will gain a higher boost than the 800 Hz filter, which is in the center of the band.

To deal with this problem, there are several different approaches. One approach is to select higher resistance potentiometers. Unfortunately, this has the effect of decreasing the linearity of the gain adjustment for the selected frequency, and making the control sensitive. Another approach would be to select a higher value resister for $R_1$, which causes the maximum gain to increase and minimum gain to decrease. We decided to implement this approach, and we set the value of $R_1$ to 1 kΩ.

### *Input stage*

One of the specifications for the equalizer circuit is the canceling of any DC offset on the input signal. Also, the source voltage should see high input impedance when looking into the circuit, so the circuit does not draw too much current from the source signal.

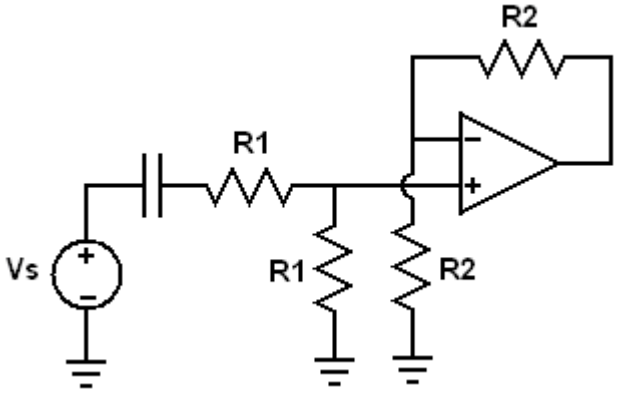


*Figure 6. Offset-canceling Input stage*

To remove any offset from the input signal, we placed a capacitor in series with the signal source. Since the DC model of a capacitor is a short circuit, the capacitor effectively removes the DC component from the source.

Next, to create high input impedance, we added a non-inverting follower circuit (see Figure 6). We chose arbitrary resister values of 1 kΩ for $R_1$ and $R_2$.

### *Output stage*

As we found it undesirable for the equalizer circuit to drain too much current from the signal source, we also decided to design a voltage follower stage for the output of the op-amp to prevent any load to load down the filters. For this stage, we simply fed the output from the equalizer into the non-inverting pin of an op-amp, and connected the inverting pin to the output pin.

# Hardware Implementation

## *Parts used and cost*

For the testing of our equalizer circuit, we implemented our design onto a breadboard. Since capacitors don't come in nominal terms as needed for our circuit in Table 1, we added available nominal values in series and parallel to crate the capacitance values needed. The nominal values, cost and quantity of all parts used in the circuit are listed in Table 2 below. All resistors are 5% ¼ watt.

| Name | Quantity | Price | Total Price |
|---|---|---|---|
| LM741 OP-AMP | 9 | 0.46 | 4.14 |
| 100 Ω Resistor | 7 | 0.09 | 0.63 |
| 510 Ω Resistor | 4 | 0.17 | 0.68 |
| 200 kΩ Resistor | 7 | 0.21 | 1.47 |
| 22 pF capacitor ceramic | 2 | 0.076 | 0.152 |
| 150 pF ceramic capacitor | 1 | 0.03 | 0.030 |
| 330 pF ceramic capacitor | 1 | 0.069 | 0.069 |
| 470 pF ceramic capacitor | 1 | 0.069 | 0.069 |
| 680 pF ceramic capacitor | 1 | 0.069 | 0.069 |
| 1 nF ceramic capacitor | 2 | 0.07 | 0.14 |
| 4.7 nF ceramic capacitor | 1 | 0.07 | 0.07 |
| 6.8 nF ceramic capacitor | 2 | 0.07 | 0.14 |
| 11 nF ceramic capacitor | 1 | 0.20 | 0.20 |
| 22 nF ceramic capacitor | 3 | 0.08 | 0.24 |
| 33 nF ceramic capacitor | 1 | 0.083 | 0.083 |
| 0.15 µF electrolytic capacitor | 1 | 0.24 | 0.24 |
| 0.33 µF electrolytic capacitor | 1 | 0.32 | 0.32 |
| 0.47 µF electrolytic capacitor | 1 | 0.162 | 0.162 |
| 0.68 µF electrolytic capacitor | 2 | 0.65 | 1.30 |
| 1 µF electrolytic capacitor | 3 | 0.077 | 0.231 |
| 4.7 µF electrolytic capacitor | 1 | 0.077 | 0.07 |
| 6.8 µF electrolytic capacitor | 2 | 0.18 | 0.36 |
| 11 µF electrolytic capacitor | 1 | 0.077 | 0.077 |
| 22 µF electrolytic capacitor | 1 | 0.077 | 0.077 |
| 33 µF electrolytic capacitor | 1 | 0.077 | 0.077 |
| 10 kΩ ¾ turn potentiometer | 7 | 0.36 | 2.52 |
| | | Total cost: | $13.62 |

*Table 2. List of parts used and cost*

# Testing

## *Test Procedure*

In order to verify the equalizer worked correctly, we devised a test procedure to verify our circuit design. The first step of the procedure involved creating models in PSpice and gathering analytical data to verify the design met the design specifications. After the design was verified, we then built the circuit and took measurements to gather experimental data. We then compared the analytical and experimental data to ensure the design was correct.

For the analytical data, we set up PSpice to simulate using an AC sweep analysis from 10 Hz to 100 kHz, recording 101 points per decade. We ran a series of three tests to verify the design met specifications before implementing the circuit using hardware. To analyze the circuit with all filter elements in, we were forced to model with series RLC circuits, since we were using an evaluation version of PSpice, which has a restriction on the number of nodes you are allowed to simulate. We refrained from adding the input and output stages for this reason. The following simulations do not account for the DC-offset canceling by the input stage, or the high frequency effects caused by the gyrator filter elements for the second and third simulation.

To gather experimental data, we set up the function generator to output a peak-to-peak signal of 1 Volt. Starting at 6.25 Hz, we recorded peak-to-peak measurements of the output signal for every quarter octave up to 102.4 kHz.

## *Analytical Data*

For our first simulation, in order to verify the correct frequency response for each of the gyrator filters, we modeled each one using PSpice in a configuration similar to Figure 4 with $R_1$ = 510 Ω. All other filters were disconnected from the circuit to prevent current from leaking through those filters. We expected the output gain for this circuit to be 6.1 V for full boost and 0.16 V for full cut (see equation 12).

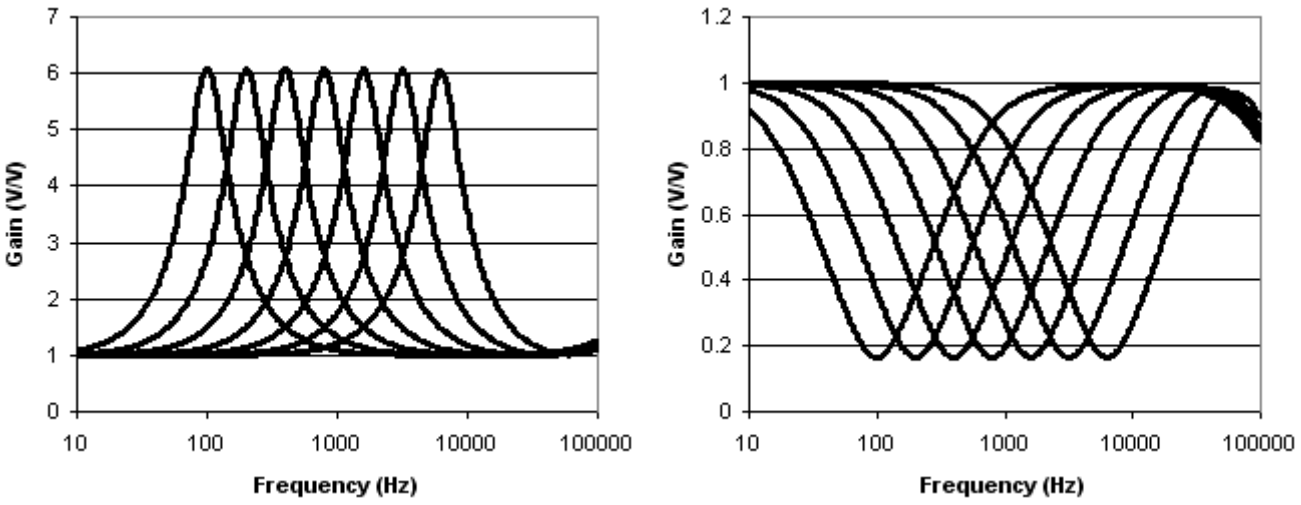


*Figure 7. Simulated frequency response of individual filters for full boost (left) and full cut (right)*

For the second simulation, we replaced $R_1$ with a 1 kΩ resistor to boost the gain, and added all components in. As discussed in the section on designing the filter configuration, each band causes parasitic filtering on other bands, reducing the amount of gain they are able to achieve.

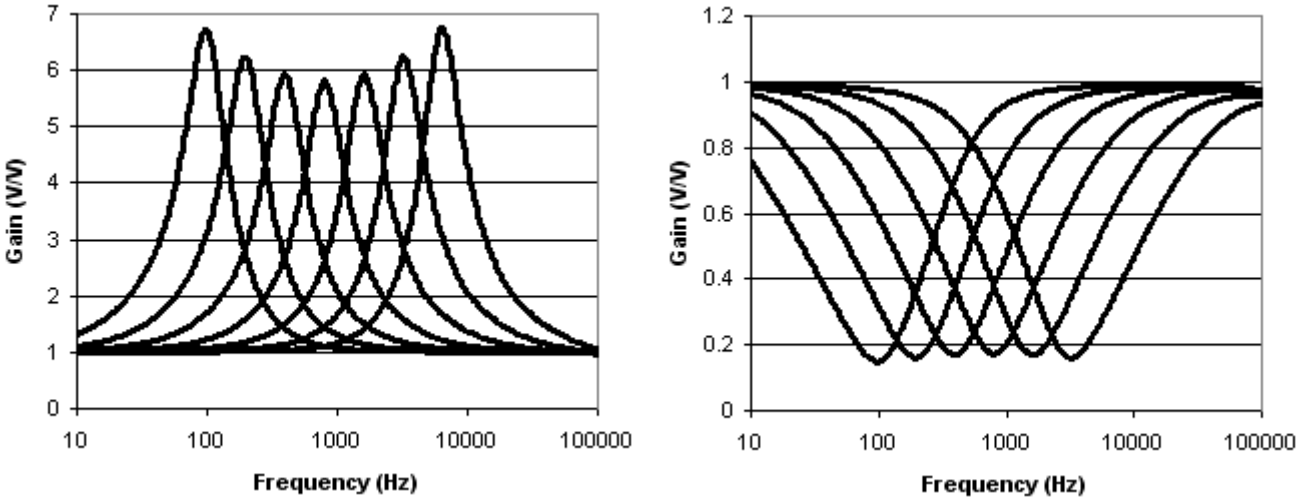


*Figure 8. Simulated frequency response of equalizer with individual filters set to full boost (left) and full cut (right)*

In our third simulation, we turned all of the filters full boost and full cut.

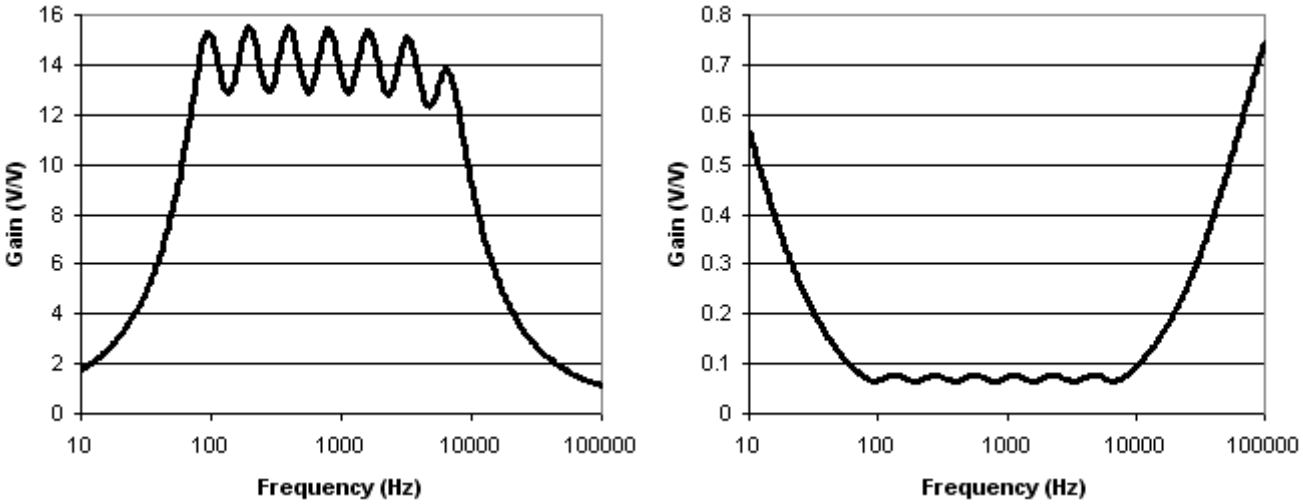


*Figure 9. Simulated frequency response of equalizer with all filters full boost (left) and full cut (right)*

## *Experimental Data*

The first two graphs show the frequency response of the individual bands at full cut and full boost. In these graphs, the DC-cancelling input stage had not yet been included in the circuit.

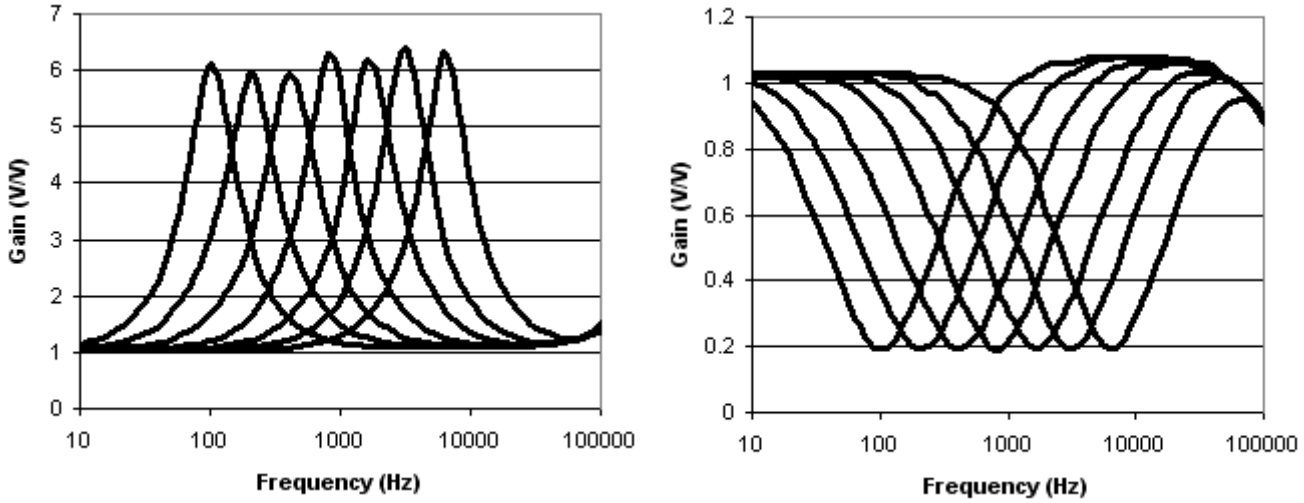


*Figure 10. Frequency response of individual filters at full boost (left) and full cut (right)*

For the next analysis, we turned all the potentiometers to full boost and to full cut, and did a frequency response analysis on the output signal. For this simulation, we included the DC cancelling input stage.

When the circuit was in full boost, at around 60 kHz, the output signal became unstable and turned into a triangle wave (see Figure 11). The triangle wave continued dropping in amplitude for higher frequencies.

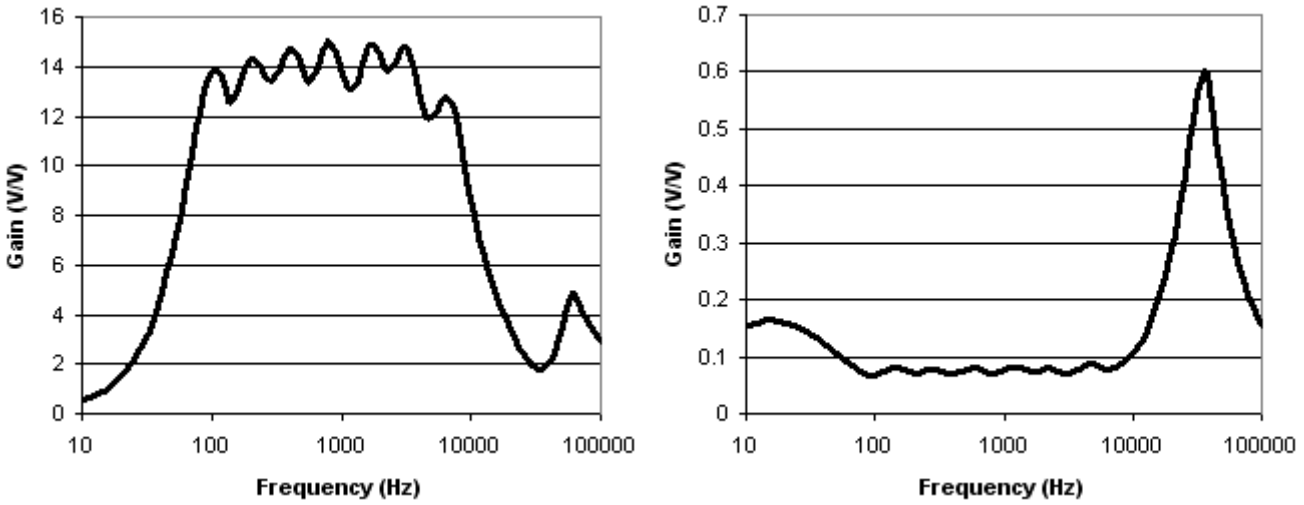


*Figure 11. Frequency response of equalizer with all filters full boost (left) and full cut (right)*

# Results

Figure 7 shows the results of the PSpice simulation for all the gyrator filters. To verify the Q values were correct, we expected the 3-dB frequencies for each filter to be at the frequency the bands intersect. The 3-dB frequency is the frequency at which the voltage of the bands is 3-dB below its maximum, which in this test should be 4.3 volts for full boost and 0.22 for full cut. Based on the results of the first simulation, we concluded the component values for our gyrator circuits were correct. The center frequencies, maximum gain and minimum gain were correct.

We also observed from our data that when the input signal get up to 60 kHz, the filters starting to draw so much current that we saw in our result a triangular wave output. This effect could be explained by the high-frequency effects of the gyrator circuit, and may be counteracted with more filtering of the output signal

The high-frequency effects apparent for frequencies over 60 kHz in Figure 11 may be due to the circuit becoming unstable when the op-amp not being able to supply enough current to feed all the filter elements. We believe this effect is caused by an unstable condition caused by the $s^2$ term in the denominator of the transfer equation (see equation 7). Further filtering may be able to eliminate this instability.

## *Parasitic Impedance Effect*

When all the filters are connected, the effect of parasitic impedance is measurable, and is evident in the output of our second PSpice simulation. When all the filters are connected to the circuit, the individual bands are not to achieve as much gain. For this reason, we changed the 510 Ω resistors with 1 kΩ resistors in order to boost the gain for the individual bands to an average of 6. The variance seen in the peaks with one filter is around 0.48 V (see Figure 7), but when the filters are all connected and turn fully on, the ripple is 2V (Figure 8). The parasitic impedance effect can be explained through the following equation that governs the total gain of the circuit:

$$\frac{E_o}{E_{in}} = \frac{1 + R / Z'_e}{1 + R / Z'_d} \qquad \textit{Equation 14}^2$$

In this equation, $Z_e'$ at full gain for a single band is just $R_4$ for a single filter. When the filter is not at full boost or cut and not within its center frequency, the impedance is at a higher impedance value $Z_e'$. The $Z_e'$ of the whole circuit is the parallel combination of all of the filters' $Z_e'$. When one band is at full gain while others are at unity, the value of $Z_e'$ for the whole circuit is always higher than the band's filter value. As Equation 14 shows, this reduces the gain of the circuit. The worst reduction is seen at the middle frequency band, which is since $Z_e'$ is the highest at this band since the band overlaps impedance seen by all their bands. So due to different parasitic impedance when different filter is on, not only does the gain get reduced, there is also a variation of gain for different frequencies.

[2] Greiner & Schoessow, p. 402 – Figure 41

One approach to reducing this effect would be to split the filters among multiple sub circuits, then sum the results together. On one circuit, you may have the 100 Hz, 400 Hz, 1600 Hz, and 6400 Hz filters, while on the other circuit, you may have the 200 Hz, 800 Hz, and 3200 Hz filters (see Figure 12). With this configuration, the bands are not as close to each other, and cause less loading on each other. Another option would be to increase the Q value, so the bands don't spread out over each other nearly as much. Still another option would be to set the bands to high gain, then add resisters in series with the potentiometers to limit the gain they can provide. Although, doing so will cause the maximum Q value of the potentiometers to vary and become too low.

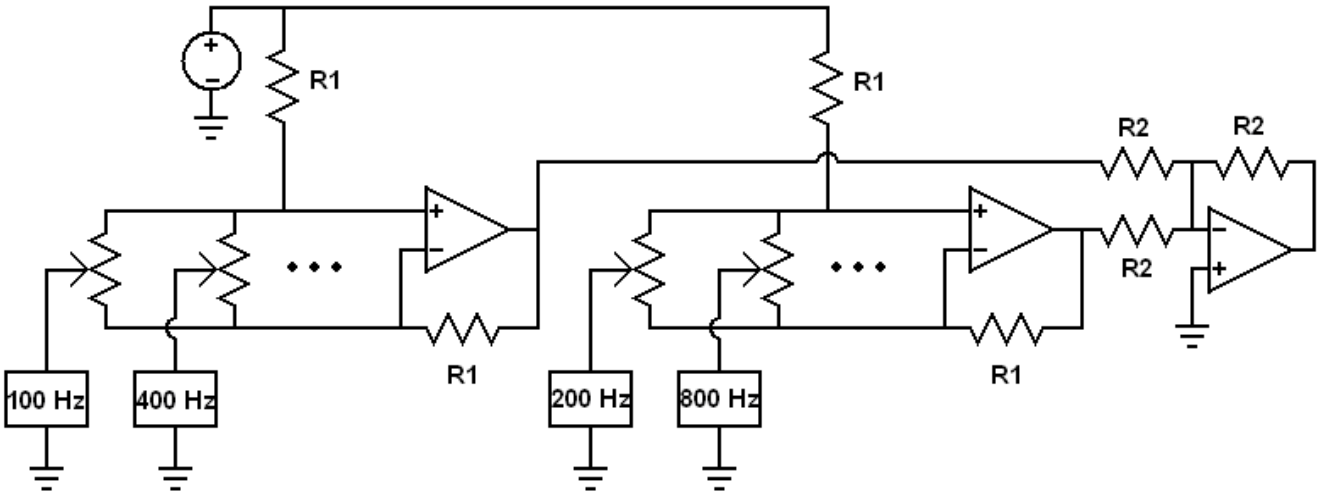


*Figure 12. Modified filter configuration*

## *Uneven Individual Band Gain*

In Figure 8, we can see that the bands all have different maximum gain, ranging from 5.92 to 6.4 for maximum boost, and from 0.196 to 0.188 for full cut. These variations in gain may be due to the mismatch in resistor and potentiometer values in each LRC filter. The gain of the circuit at full boost and cut requires the potentiometer to be able to vary its resistance from 0 to its rated value. This at full boost results in a gain (see equation 13).

In this equation, $R_1$ is the feedback resistor and $R_4$ the resistive element in the filter. In reality, potentiometers cannot go all the way to 0 or all the way up to its maximum value, making the gain at full boost depends dependant on the values if $R_2$ and $R_3$ (see equation 12).

From equation 12, we can see that if $R_3$ is not equal to 0, it will reduce the maximum boost and cut for the filter, which may explain the variation of the peak gains in Figure 10. Also, the resistive element in the filters determines the gain and cut of the equalizer. If the actual value $R_4$ is at a value higher than the rated value, we will get a lower gain at full boost, and if the value is lower we will get a higher boost, which is again what we saw in some of the filters.

# Conclusion

In this project, we described the design and testing process for our graphic equalizer design. Overall, our design met most of the design specification within an acceptable margin of error. Design  The graphic equalizer we designed is very robust to low frequency noise, which is due to the decoupling capacitors we placed at the supply rail. We analyzed the use of gyrators in filter elements can closely match the use of LRC filters for lower frequencies. One of them is to get more precise resistor values. Another is to reduce the current load the output amplifier has to handle by separating the equalizer into two or more equalizers in series. By doing this, the individual bands of the equalizer see less parasitic impedance by the other equalizer bands. These improvements can improve the accuracy of the gain and reduce the ripple voltage of the equalizer. By separating the equalizer into separate sections (see Figure 12), not only does the current require from the output amplifiers less, it also allows us to reduce the value of the potentiometer. By reducing the value of the potentiometer, $Z_e'$ from Equation 14 would be closer to the desired single filter value due to the value of the parasitic impedance of the other filters is greatly contribute by the value of the potentiometer.

# References

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